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MULTI-CHANNEL SERDES RECEIVER FOR CHIP-TO-CHIP AND BACKPLANE INTERCONNECTS AND METHOD OF OPERATION THEREOF

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MULTI-CHANNEL SERDES RECEIVER FOR CHIP-TO-CHIP AND BACKPLANE INTERCONNECTS AND METHOD OF OPERATION THEREOF

TECHNICAL FIELD OF THE INVENTION

[0001] The present invention is directed, in general, to serializer/deserializer ("serdes") circuits and, more specifically, to a multi-channel serdes receivers for chip-to-chip and backplane interconnects and a method of operating the same.

BACKGROUND OF THE INVENTION

[0002] As technology continues to advance at an unprecedented rate, the transfer of information or data has remained a high priority. In addition, as processing speeds continue to increase, the speed at which information is transferred remains key in increasing overall system speed. Traditionally, parallel busses or cables have been coupled between multiple devices to transfer information during a processing function. However, problems that may degrade the data transferred, such as signal loss when transmitted over long distances, have led to improvements in the manner in which such data is transferred. In addition, the multitude of wires or cables necessary for parallel connection may become cumbersome, especially in larger systems. In the past,

however, alternatives to parallel connections often led to information bottlenecks, leaving parallel lines as the only viable choice.

[0003] As the need for bandwidth expands in the various networks now existing, or even those later developed, serial backplanes (or busses) have become the ideal alternative for solving these problems. Typically, serial backplanes employ a serializer at a transmitting end to convert and transmit data in serial order and a deserializer at a receiving end to convert the data back to parallel form once received. Such serializer/deserializer ("serdes") receivers have become the benchmark for asynchronous communication and have provided clear advantages over parallel busses. For example, serdes receivers include transmitters and receivers, and use simplified wiring harnesses (often only a single wire per channel) that typically consume less power than their parallel-coupled counterparts. Higher performance may also be achieved because serdes receivers reduce the crosstalk that often occurs between parallel wires. In addition, serdes receivers may be employed to transmit data over long distances without the signal degradation experienced with parallel busses ultimately offering increased reliability and fidelity over parallel busses.

[0004] Although a tremendous improvement over parallel busses, serial connections employing serdes receivers are not without problems. Since a separate clock signal for component and signal

synchronizing is not used (typical of asynchronous communication), the receiving and transmitting ends of a serdes are synchronized by monitoring the transmitted data. Within a conventional serial bus, each line of communication includes a separate serdes transceiver, each having a serdes receiver and transmitter, for serializing and deserializing each flume of data. As a result, each serdes receiver includes its own phase-locked loop (PLL) circuit, each typically employing a voltage controlled oscillator (VCO) to generate the clock at the receiving end of the data transmission and to synchronize the clock with the timing of the data signal at the transmitting end. Without this synchronization, the data transmitted would likely be corrupted or lost.

[0005] Among the more prominent problems typically found in conventional serial busses is the occurrence of crosstalk between VCOs in each of the serdes receivers. This crosstalk often results in skewed timing of the clocks, as well as jitter in the VCOs themselves. In addition, since each of the VCOs uses power to operate, the combined operation of multiple VCOs results in relatively large power consumption for the system.

[0006] Accordingly, what is needed in the art is a serdes receiver for use with a serial bus that does not suffer from the problems and deficiencies found in the prior art.

SUMMARY OF THE INVENTION

[0007] To address the above-discussed deficiencies of the prior art, the present invention provides a multi-channel serdes receiver, a method of operating the receiver and an integrated circuit configured as a serdes receiver. In one embodiment, the receiver includes: (1) a PLL-based central frequency synthesizer and (2) a plurality of channel-specific receivers coupled to the central frequency synthesizer, each of the plurality including a clock recovery system having a phase detector and a phase interpolator, the clock recovery system coupling the phase detector and the central frequency synthesizer.

[0008] The present invention therefore introduces a multi-channel serdes receiver built around a central frequency synthesizer (clock) and distributed clock and data recovery in each channel-specific receiver. The clock and data recovery circuit in each channel-specific receiver tracks the frequency offset between the incoming data's clock and the clock generated by the central frequency synthesizer ("PLL"). The multi-channel serdes receiver presented here is capable of tolerating frequency offset between a plurality of channels. Centralizing the clock reduces interference that occurs when multiple frequency synthesizers run proximate one another and reduces power consumption and concomitant heat generation, which is particularly important when the serdes

receiver is embodied as an integrated circuit.

[0009] In one embodiment of the present invention, the central frequency synthesizer includes a voltage-controlled oscillator. Those skilled in the pertinent art will understand that other types of frequency synthesizers are within the broad scope of the present invention.

[0010] In one embodiment of the present invention, the central frequency synthesizer is a phase-locked loop (PLL). The phase-locked loop, while not essential to the present invention, improves the stability and reliability of the central frequency synthesizer.

[0011] In one embodiment of the present invention, the plurality further includes at least one integrator coupled to the phase interpolator and a demultiplexer. In a more specific embodiment, the at least one integrator performs an integrate-and-dump function. The structure and function of the at least one integrator and the demultiplexer will be described in greater detail in the Detailed Description that follows.

[0012] In one embodiment of the present invention, the phase interpolator and the phase detector comprise a delay-locked loop (DLL). One possible architecture for a such a delay-locked loop is set forth in U.S. Patent Application Serial No. [Attorney Docket No. LARSSON _-_], entitled "Four Quadrant Analog Mixer-Based Delay-Locked Loop (DLL) for Clock and Data Recovery," which is incorporated herein by reference.

[0013] In one embodiment of the present invention, the central frequency synthesizer provides both in-phase and quadrature-phase clock signals.

[0014] The foregoing has outlined, rather broadly, preferred and alternative features of the present invention so that those skilled in the art may better understand the detailed description of the invention that follows. Additional features of the invention will be described hereinafter that form the subject of the claims of the invention. Those skilled in the art should appreciate that they can readily use the disclosed conception and specific embodiment as a basis for designing or modifying other structures for carrying out the same purposes of the present invention. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the invention in its broadest form.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] For a more complete understanding of the present invention, reference is now made to the following detailed description taken in conjunction with the accompanying FIGUREs. It is emphasized that various features may not be drawn to scale. In fact, the dimensions of various features may be arbitrarily increased or reduced for clarity of discussion. In addition, it is emphasized that some circuit components may not be illustrated for clarity of discussion. Reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0016] FIGURE 1 illustrates a block diagram of a multi-channel serdes receiver constructed according to the principles of the present invention;

[0017] FIGURE 2 illustrates a block diagram of one embodiment of the front end 1:4 demultiplexer of a multi-channel serdes receiver manufactured according to the principles of the present invention;

[0018] FIGURE 3 illustrates a timing diagram of the 1:4 deserializing operation performed by the front end of a serdes receiver of the present invention;

[0019] FIGURE 4 illustrates a block diagram of one embodiment of the clock generation circuit discussed with respect to FIGURE 2;

[0020] FIGURE 5 illustrates a timing diagram of waveforms

demonstrating the quadrature phase relationship between first and second in-phase signals and first and second quadrature phase signals;

[0021] FIGURE 6 illustrates one embodiment of first and second synchronizing circuits discussed with respect to FIGURE 4; and

[0022] FIGURE 7 illustrates a timing diagram of waveforms representing the several signals shown in the clock generating circuit 260 of FIGURE 4.

DETAILED DESCRIPTION

[0023] Referring initially to FIGURE 1, illustrated is a block diagram of a multi-channel serdes receiver 100 constructed according to the principles of the present invention. As illustrated, the receiver 100 includes N (an arbitrary number of) channel-specific receivers, Ch1, Ch2 ... ChN, which correspond directly to the number of channels desired. Those skilled in the art understand that a separate channel may be used for each data transmission stream desired. Although only the components of the first channel, Ch1, are illustrated in detail, it should be understood that the channel-specific receivers for the second through the Nth channels include similar components. However, those components are not discussed here in detail in order to avoid repetition.

[0024] Unlike serdes receivers found in the prior art, the serdes receiver 100 of the present invention includes only a single PLL circuit 105. The PLL circuit 105 includes a central frequency synthesizer, which, in an advantageous embodiment, is a VCO. The PLL circuit 105 employs the central frequency synthesizer to generate an in-phase signal, I, and a quadrature phase signal, Q, based on a reference signal S_{ref}. In one embodiment, the reference signal S_{ref} is a master clock signal for use by surrounding circuits and components, including the serdes receiver 100. As shown in

FIGURE 1, the in-phase and quadrature phase signals, I and Q, are then provided to the channel-specific receivers, CH1, Ch2, ChN, of the serdes receiver 100 for use in deriving a clock signal for each of the channels. Derivation of a clock signal for the first channel Ch1 will now be described in greater detail. (Derivation of the clock signal is identical for each of the multiple channels of the serdes receiver 100.)

[0025] The in-phase and quadrature phase signals, I and Q, are provided to a phase interpolator 110. Though not necessary to the broad scope of the present invention, the phase interpolator 110 in the illustrated embodiment is an analog mixer-based phase interpolator. A first input signal S_{in-1} is provided to a clock generation circuit 135, and then to a phase detector (PD) 115. An output of the PD 115 is provided to the phase interpolator 110 along with the in-phase and quadrature phase signals, I and Q. The function of the clock generation circuit 135 will be discussed in detail with reference to FIGUREs 2 and 3. The phase interpolator 110, together with the phase detector 115, comprise a delay-locked loop (DLL), such as the DLL described in co-pending patent application number [Attorney Docket No. LARSSON _-_], filed on [filing date], entitled "Four Quadrant Analog Mixer-Based Delay-Locked Loop for Clock and Data Recovery," and incorporated herein by reference. The benefits and advantages of clock and data recovery using a DLL circuit of the type described therein are

discussed in detail in the co-pending application, so that discussion will not be repeated here.

[0026] In the illustrated embodiment, the input signal S_{in} represents the data transmitted to the serdes receiver 100 through a serial line. Of course, to other multiple channels Ch2, ChN, of the serdes receiver 100 receives an input signal S_{in-2}, S_{in-N} unique to each particular channel Ch2, ChN. The PD 115 is employed to compare a phase of the first input signal S_{in} to the recovered clock, and that result is used to determine the output of the PD 115 used by the phase interpolator 115 to perform clock and data recovery for the first channel Ch1.

[0027] An output of the phase interpolator 110 is then fed back to the PD 115. That feedback output is used by the PD 115, in addition to the first input signal S_{in-1}, to derive and generate the output of the PD 115. The output of the phase interpolator 110, which will be discussed in greater detail below, is also provided to first and second integrators 120, 125. Also, the first input signal S_{in-1} is provided to the first and second integrators 120, 125 for use in the deserialization process. The outputs of the first and second integrators 120, 125 are provided to a demultiplexer 130. The demultiplexer 130 provides a final step in the deserialization process and the output of the demultiplexer 130 is the data in parallel form.

[0028] With this broad description, it is clear that the present

invention introduces a multi-channel serdes receiver built around a central frequency synthesizer (clock) and distributed clock and data recovery circuits in each channel. By removing the separate clocks from each of the channel-specific receivers, Ch1, Ch2, ChN, and centralizing the clock, interference that typically occurs when multiple frequency synthesizers run proximate one another may be reduced. In addition, power consumption and concomitant heat generation, which is particularly important when the serdes receiver 100 is embodied as an integrated circuit, may also be reduced.

[0029] Turning now to FIGURE 2, illustrated is a block diagram of one embodiment of the front end 200 of a multi-channel serdes receiver manufactured according to the principles of the present invention. In the illustrated embodiment, the front end 200 represents a 1:4 deserialization (demultiplexing) of an incoming serial data signal S_{in}. Those skilled in the art understand that a serdes receiver according to the present invention may provide other ratios for deserializing data signals, and the present invention is not limited to any particular ratio.

[0030] To perform the 1:4 deserializing, a 1:2 deserialization is first realized through first and second integrators 210, 215. The first and second integrators 210, 215 are controlled respectively by first and second waves Ck_{1a}, Ck_{1b} of a recovered half-rate clock signal (collectively Ck) generated by a clock and

data recovery circuit (CDR) 205 and a clock generation circuit 260. In an advantageous embodiment, the integrators 210, 215 in FIGURE 2 perform an integrating and dumping function by integrating the first input signal S_{in-1} over a one-bit period and then resetting to zero.

[0031] To finish the 1:4 deserializing of the first input signal S_{in-1}, a second 1:2 deserializing step is then performed. More specifically, the first integrator output S_A is further deserialized by a factor of 2 through first and second switches 220, 225. Likewise, the second integrator output S_B is also deserialized by a factor of 2 by third and fourth switches 230, 235. In a more specific embodiment, the switches 220, 225, 230, 235 are "sample and hold" switches, however any suitable switching device may be employed to further deserialize/demultiplex the first input signal S_{in-1} in accordance with the principles described herein.

[0032] The first and second switches 220, 225 are controlled by first and second waves Ck_{2ia}, Ck_{2ib} of a divided-by-two in-phase recovered half-rate clock signal (collectively Ck_{2i}) generated by the clock generation circuit 260. Similarly, the third and fourth switches 230, 235 are controlled by first and second portions Ck_{2qa}, Ck_{2qb} of a divided-by-two quadrature phase clock signal (collectively Ck_{2q}) also generated by the clock generation circuit 260. In the illustrated embodiment of the front end 200, the in-

phase and quadrature clock signals Ck_{2ia}, Ck_{2ib}, Ck_{2qa}, Ck_{2qb} are divide-by-two clocks derived from the recovered half-rate clock signal Ck. Of course, the source of the in-phase and quadrature phase recovered half-rate clock signals Ck_{2ia}, Ck_{2ib}, Ck_{2qa}, Ck_{2qb} may be different depending on the desired operation of the front end 200 of the serdes receiver.

[0033] To complete the 1:4 deserializing of the first input signal S_{in-1}, the four outputs of the switches 220, 225, 230, 235 are regenerated using first, second, third and fourth latches 240, 245, 250, 255. The latches 240, 245, 250, 255 generate first, second, third and fourth output signals S_{out1}, S_{out2}, S_{out3}, S_{out4}. The output signals S_{out1}, S_{out2}, S_{out3}, S_{out4} represent the parallel data signals typically found in equipment communicating with a parallel backplane. Turning briefly to FIGURE 3, illustrated is a timing diagram 300 of the 1:4 deserializing operation performed by the front end 200 of a serdes receiver of the present invention.

[0034] Referring now to FIGURE 4, illustrated is a block diagram of one embodiment of the clock generation circuit 260 discussed with respect to FIGURE 2. As illustrated, a divider 405 divides-by-two first and second recovered clock signals Ck_a, Ck_b (Ck_a, Ck_b are complimentary and may be denoted collectively as Ck) to generate first and second non-synchronized in-phase signals $CkNS_{2ia}$, $CkNS_{2ib}$ and first and second non-synchronized quadrature phase signals $CkNS_{2qa}$, $CkNS_{2qb}$. In an exemplary embodiment, the non-

synchronized first and second in-phase signals $CkNS_{2ia}$, $CkNS_{2ib}$ and non-synchronized first and second quadrature phase signals $CkNS_{2qa}$, $CkNS_{2qb}$ have a quadrature phase relationship. Turning briefly to FIGURE 5, the waveforms illustrated therein exhibit this phase relationship.

[0035] Returning to FIGURE 4, also illustrated are first and second synchronizing circuits Sync1, Sync2. In this embodiment, the second synchronizing circuits Sync2 are used to re-synchronize the non-synchronized first and second in-phase signals $CkNS_{2ia}$, $CkNS_{2ib}$ and the non-synchronized first and second quadrature phase signals $CkNS_{2qa}$, $CkNS_{2qb}$ with the first and second recovered clock signals Ck_a, Ck_b. The synchronization is performed by using the first and second recovered clock signals Ck_a, Ck_b to sample the non-synchronized first and second in-phase signals $CkNS_{2ia}$, $CkNS_{2ib}$ and the non-synchronized first and second quadrature phase signals $CkNS_{2qa}$, $CkNS_{2qb}$. The synchronizing circuits Sync1, Sync2 and sampling are illustrated in FIGURE 6.

[0036] To have true synchronized clocks, the first synchronizing circuit Sync1 is added into the signal path of the first and second recovered clock signals Ck_a, Ck_b in order to match the delay introduced by the second synchronizing circuits Sync2. In this particular embodiment, since the first and second synchronizing circuits Sync1, Sync2 have substantially the same circuit topology and signal path (see FIGURE 6), the delays associated with the

synchronizing circuits Sync1, Sync2 are matched. Looking at FIGURE 7, illustrated is a timing diagram 700 of waveforms representing the several signals associated with the clock generation circuit 260 of FIGURE 4. The relationships between the original recovered clock signals Ck_a, Ck_b, the non-synchronized in-phase and quadrature phase signals $CkNS_{2ia}$, $CkNS_{2ib}$, $CkNS_{2qa}$, $CkNS_{2qb}$, the synchronized in-phase and quadrature phase signals CkS_{2ia}, CkS_{2ib}, CkS_{2qa}, CkS_{2qb}, and the final signals Ck_a, Ck_b, Ck_{2ia}, Ck_{2ib}, Ck_{2qa}, Ck_{2qb} output from buffers 440-465 coupled to the first and second synchronizing circuits Sync1, Sync2 are illustrated therein.

[0037] By building a multi-channel serdes receiver around a central frequency synthesizer and distributed clock and data recovery systems for each channel, the present invention provides several notable advantages over the prior art. For instance, the present invention provides for removing the separate clocks from all channel-specific receivers and centralizing the clock, reducing interference that typically occurs when multiple frequency synthesizers run proximate one another. Power consumption and concomitant heat generation is also reduced with this configuration, which is particularly important when the serdes receiver is embodied as an integrated circuit. Those skilled in the art understand that reducing the number of frequency synthesizers within a serdes receiver allows for more efficient power consumption, as well as reducing or eliminating the chance

for crosstalk and jitter. Moreover, a serdes receiver, as well as a method of operating a serdes receiver, according to the principles of the present invention is employable in almost any environment where asynchronous communication using serial busses or backplanes is desirable, while retaining benefits such as those described above.

[0038] Although the present invention has been described in detail, those skilled in the art should understand that they can make various changes, substitutions and alterations herein without departing from the spirit and scope of the invention in its broadest form.